P1: Draw a schematic and layout for a bit slice of the 8-bit counter. Using the bit-slice, construct the 8-bit counter. DRC, LVS and SPECTER simulate the extracted counter.

P2. Using Verilog HDL only, design the 8-bit binary counter, constructed from gate level primitives (NAND, NOR, INV, COMPLEX Gates, etc …). That is, write the behavioral models for the primitives and construct the counter in schematic. Assume that a single INV (2 transistors) have a delay of 1ns. For each series transistor in the pull-up or pull-down networks of your gates, include a delay of 0.5ns. Each parallel transistor does not alter the base response time of the gate (because they add as much capacitance as current). That is, a CMOS NOR gate would have a fall time of 0.5ns, but a rise time of 1ns. Run the Verilog simulation of the counter, showing all the states. Determine the longest delay path for the counter. Determine the maximum frequency of the counter. Does the maximum frequency consistent with the longest delay path. Explain.

P3. Redesign your counter to include a “Direction” bit. This bit will make the counter to either count up or count down. Demonstrate the counter working with SPICE simulations of the schematic (layout and Verilog are not required for this problem). Determine the maximum speed and power consumption for the new counter.