Tips on IC layout
A Typical Digital Circuit layout
Design Flow
Drawing a single transistor

Make sure to put multiple contacts for large transistors
Compact Your Transistors

L = 0.2μm
W = 20μm

L = 0.2μm
W = 5μm

L = 0.2μm
W = 5μm

L = 0.2μm
W = 5μm

L = 0.2μm
W = 5μm
Compact Your Transistors

Split into 4 transistors

Flip 2nd and 4th transistors

Compact the transistors

5um
Use multiple fingers for your transistors
Transistor Parasitic Capacitance

- $jsw$: junction side-wall capacitance
- $j$: junction capacitance
- $gb$: gate to bulk
- $db$: drain to bulk
- $sb$: source to bulk
Avoid Extra Parastic

Poor Layout

Capacitance between the metal and the poly, and between the poly and the substrate makes the transistors operate slower.

Improved Layouts

Use of multiple contacts per gate happen to join up the gates.
Leave plenty of extra space

End-of-Line has higher variation in etch rate
Testing the actual circuit
Cadence Short Cuts

1 (lowercase L): create a wire name
f: fit everything in the screen
z: zoom by clicking 2 points specifying the selection box
TAB: center the screen on the next mouse click (centers where you click the mouse)
CTRL z: zoom in
SHIFT z: zoom out
x: descend into a cell
b: ascend out of a cell
u: undo, U: redo
s: stretch the object (very useful in layouts)
m: move the object
r: rotate (in schematic) – create rectangle (in layout)
i: insert instance/cell
c: copy
CTRL d: deselect (very useful in layouts when have large cells)
k: create ruler, SHIFT k: remove all rulers
Reference

• http://www.eda-utilities.com/CMOS_Transistor_Layout_KungFu.pdf